What is claimed is:

1. A method for fabricating a metal-oxide semiconductor (MOS) transistor, comprising the steps of:

(a) forming sequentially a first oxide layer and a first nitride layer on a substrate;

(b) forming a device isolation layer filled in a first trench formed by selectively etching the first oxide layer, the first nitride layer and a first portion of the substrate;

(c) forming a second trench defining a channel region therebeneath by selectively etching the first oxide layer, the first nitride layer and a second portion of the substrate;

(d) forming a gate oxide layer on lateral sides and a bottom side of the second trench; and

(e) forming a gate electrode on the gate oxide layer.

2. The method as recited in claim 1, wherein the step (e) includes the steps of:

(e1) depositing a polysilicon layer for forming a gate electrode on an entire surface of the substrate;

(e2) performing a CMP process to the polysilicon layer for forming the gate electrode until the device isolation oxide layer is exposed;

(e3) depositing a tungsten nitride barrier layer, a tungsten layer for forming a gate electrode and a second nitride layer on an entire surface of the substrate;

(e4) patterning the second nitride layer, the tungsten

layer for forming the gate electrode and the tungsten nitride barrier layer into a predetermined gate electrode pattern;

(e5) forming a lateral nitride layer at lateral sides of the patterned tungsten nitride barrier layer and the tungsten layer for forming the gate electrode with a thin thickness; and

(e6) etching an exposed portion of the polysilicon layer for forming the gate electrode and performing a selective oxidation process thereto so that a selective oxide layer is grown only at a portion of the substrate and lateral sides of the exposed polysilicon layer not being buried in the second trench.

3. The method as recited in claim 1, after the step (c), further comprising the steps of:

(c1) forming a buffer oxide layer on the substrate;

(c2) performing a channel ion-implantation technique to the second trench for defining the channel region; and

(c3) removing the first nitride layer and the buffer oxide layer.

4. The method as recited in claim 1, wherein the first oxide layer has a thickness ranging from about 5 nm to about 20 nm and the first nitride layer has a thickness ranging from about 50 nm to about 150 nm.

5. The method as recited in claim 1, wherein the first

trench is formed with a depth in a range from about 150 nm to about 400 nm.

6. The method as recited in claim 1, further comprising the step of forming a sacrificial oxide layer or a thermal oxide layer at lateral sides and a bottom side of the trench prior to the formation of the device isolation oxide layer and etching the sacrificial oxide layer or the thermal oxide layer.

7. The method as recited in claim 1, further comprising the step of forming a p-type well and an n-type well at each predetermined region after forming the device isolation oxide layer.

8. The method as recited in claim 3, wherein the channel ion-implantation technique is performed with energy ranging from about 1 KeV to about 100 KeV.

9. The method as recited in claim 1, wherein the gate oxide layer has a thickness ranging from about 3 nm to about 10 nm.

10. The method as recited in claim 2, wherein the polysilicon for forming the gate electrode is formed in a thick thickness ranging from about 50 nm to about 400 nm.

11. The method as recited in claim 2, wherein the

tungsten nitride barrier layer, the tungsten layer for forming the gate electrode and the second nitride layer have a thickness in a range from about 3 nm to about 10 nm, in a range from about 50 nm to about 150 nm and in a range from about 150 nm to about 400 nm, respectively.

12. The method as recited in claim 2, wherein the barrier layer can use TiN, WSiN, TiSiN or WSi_x instead of using WN.

13. The method as recited in claim 2, wherein the lateral nitride layer has a thickness ranging from about 3 nm to about 40 nm.

14. The method as recited in claim 2, wherein the selective oxide layer has a thickness ranging from about 1.5 nm to about 10 nm.

15. The method as recited in claim 2, further comprising the step of depositing a nitride layer on an entire surface of the substrate and the gate electrode after growing the selective oxide layer in order to prevent losses of the selective oxide layer formed at lateral sides of the exposed portion of the polysilicon layer for forming the gate electrode.

16. The method as recited in claim 15, wherein the

nitride layer has a thickness ranging from about 5 nm to about 40 nm.

17. The method as recited in claim 2, after the step (e6), further including the step of forming a lateral nitride layer by depositing a nitride layer with a thin thickness and subsequently etching the nitride layer so that the selective oxide layer can be protected from any damage or loss.

18. A method for fabricating a metal-oxide semiconductor (MOS) transistor, comprising the steps of:

forming sequentially a first oxide layer and a first nitride layer on a substrate;

etching selectively the first nitride layer and the first oxide layer to expose a portion of the substrate;

etching the exposed portion of the substrate with a predetermined thickness to form a first trench at a device isolation region;

depositing a device isolation oxide layer on an entire surface of the substrate in such a manner that the device isolation layer is filled into the first trench;

performing a chemical mechanical polishing (CMP) process until the first nitride layer is exposed;

etching selectively the first nitride layer except for the exposed portion of the first nitride layer and the first oxide layer with use of a mask pattern for forming a predetermined gate electrode;

etching an exposed portion of the substrate with a predetermined thickness to form a second trench defining a channel region and clean the trench;

forming a buffer oxide layer on the substrate;

performing a channel ion-implantation technique to the second trench defining the channel region;

removing the first nitride layer and the buffer oxide layer and growing a gate oxide layer on lateral sides and a bottom side of the exposed portion of the substrate;

depositing a polysilicon layer for forming a gate electrode on an entire surface of the substrate;

performing a CMP process to the polysilicon layer for forming the gate electrode until the device isolation oxide layer is exposed;

depositing a tungsten nitride barrier layer, a tungsten layer for forming a gate electrode and a second nitride layer on an entire surface of the substrate;

patterning the second nitride layer, the tungsten layer for forming the gate electrode and the tungsten nitride barrier layer into a predetermined gate electrode pattern;

forming a lateral nitride layer at lateral sides of the patterned tungsten nitride barrier layer and the tungsten layer for forming the gate electrode; and

performing a selective oxidation process to form and grow a selective oxide layer on the polysilicon layer for forming the gate electrode encompassed by the substrate and the lateral nitride layer in order to recover any damage generated

by the etch process.